

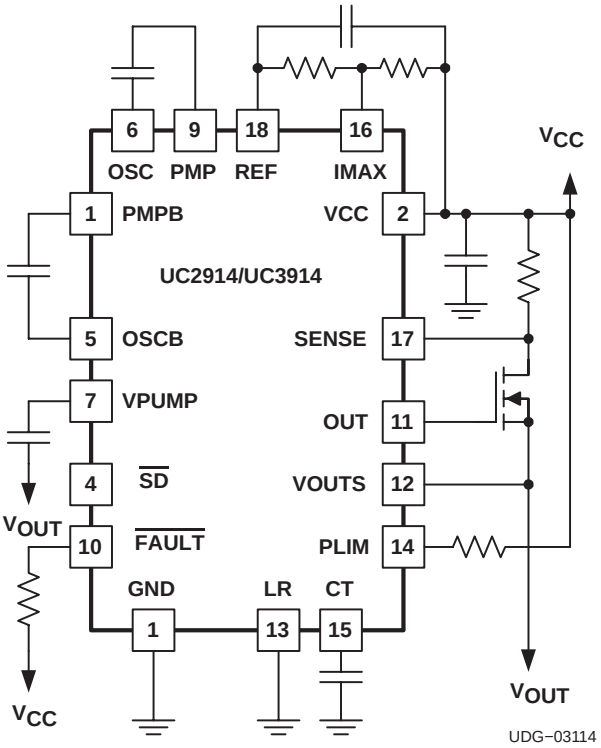
SLUS425C − DECEMBER 2003 − REVISED JULY 2004

5-V to 35-V HOT SWAP POWER MANAGER

FEATURES

- 5-V to 35-V Operation
- Precision Maximum Current Control
- Precision Fault Threshold
- Programmable Average Power Limiting
- Programmable Overcurrent Limit
- Shutdown Control
- Charge Pump for Low $R_{DS(on)}$ High-Side Drive
- Latch Reset Function Available
- Output Drive V_{GS} Clamping
- Fault Output Indication
- 18-Pin DIL and SOIC Packages

SIMPLIFIED APPLICATION DIAGRAM



DESCRIPTION

The UC3914 family of hot swap power managers provides complete power management, hot swap and fault handling capability. Integrating this part and a few external components, allows a board to be swapped in or out upon failure or system modification without removing power to the hardware, while maintaining the integrity of the powered system. Complementary output drivers and diodes have been integrated for use with external capacitors as a charge pump to ensure sufficient gate drive to the external N-channel MOSFET transistor for low $R_{DS(on)}$. All control and housekeeping functions are integrated and externally programmable and include the fault current level, maximum output sourcing current, maximum fault time and average power limiting of the external FET. The UC3914 features a duty ratio current limiting technique, which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. The fault level is fixed at 50 mV with respect to VCC to minimize total dropout.

The fault current level is set with an external current sense resistor. The maximum allowable sourcing current is programmed by using a resistor divider from VCC to REF to set the voltage on IMAX. The maximum current level, when the output appears as a current source is $(V_{VCC} - V_{IMAX})/R_{SENSE}$.

This part is offered in both 18-pin DW wide-body (SOIC) and dual-in-line (DIL) packages.

PRODUCT PREVIEW



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DESCRIPTION (continued)

When the output current is less than the fault level, the external output transistor remains switched on. When the output current exceeds the fault level, but is less than the maximum sourcing level programmed by IMAX, the output remains switched on, and the fault timer starts to charge C_T, a timing capacitor. Once C_T charges to 2.5 V, the output device is turned off and C_T is slowly discharged. Once C_T is discharged to 0.5 V, the device performs a retry and the output transistor is switched on again. The UC3914 offers two distinct reset modes. In one mode with LR left floating or held low, the device tries to reset itself repeatedly if a fault occurs as described above. In the second mode with LR held high, once a fault occurs, the output is latched off until either LR is toggled low, the part is shutdown then re−enabled using $\overline{SD}$, or the power to the part is turned off and then on again.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted.(1)(2)

		UC2914 UC3914	UNIT
Input supply voltage	VCC	40	V
Maximum forced voltage	$\overline{SD}$, LR	12	V
	IMAX	VCC	V
Maximum current	$\overline{FAULT}$	20	mA
	PLIM	10	mA
Maximum voltage	$\overline{FAULT}$	40	V
Reference output current		internally limited	A
Storage temperature range, T_{stg}		−65 to 150	°C
Junction temperature range, T_J		−55 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability

(2) Currents are positive into and negative out of the specifief terminal unless otherwise noted. All voltage values are with respect to the network ground terminal.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			5		35	V
Operating free-air temperature range, T_A	UC2914		−40		85	°C
	UC3914		0		70	°C

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C for the UC3914, −40°C to 85°C for the UC2914, V_{CC} = 12V, V_{PUMP} = $V_{PUMP(max)}$, $\overline{SD}$ = 5 V, C_{P1} = C_{P2} = C_{PUMP}= 0.01 µF. T_A = T_J. (Unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{CC}	Supply current(2)			8	15	mA
		V_{CC} = 35 V		12	20	
I_{CCSD}	Shutdown supply current	$\overline{SD}$ = 0 V,		500	900	µA
	UVLO turn−on threshold voltage			4.0	4.4	V
	UVLO hysteresis		55	120	250	mV
FAULT TIMING						
	Overcurrent threshold	T_J = 25°C, wrt V_{CC}	−55	−50	−45	mV
		Over operating temperature wrt V_{CC}	−57	−50	−42	
	IMAX input bias			1	3	µA
I_{CT_CHG}	CT charge current	V_{CT} = 1 V	−140	−100	−60	
		V_{CT} = 1 V, overload condition	−6.0	−3.0	−1.5	mA
I_{CT_DSCH}	CT discharge current	V_{CT} = 1 V	2.0	3.0	4.5	µA
V_{CT_FLT}	CT fault threshold voltage		2.25	2.50	2.75	V
V_{CT_RST}	CT reset threshold voltage		0.45	0.50	0.55	
	Output duty cycle	Fault condition, I_{PL} = 0 A	1.5%	3.0%	4.5%	
OUTPUT						
V_{OH}	High-level output voltage	V_{VOUTS} = V_{CC}, V_{PUMP} = $V_{PUMP(max)}$, wrt V_{PUMP}	−1.5	−1.0		V
		V_{VOUTS} = V_{CC}, V_{PUMP} = $V_{PUMP(max)}$, I_{OUT} = −2 mA, wrt V_{PUMP}	−2.0	−1.5		
V_{OL}	Low-level output voltage	I_{OUT} = 0 A		0.8	1.3	
		I_{OUT} = 5 mA		1	2	
		I_{OUT} = 25 mA, overload condition V_{VOUTS} = 0 V		1.2	1.8	
$V_{OUT(cl)}$	Output clamp voltage	V_{OUTS} = 0 V	11.5	13.0	14.5	
t_{RISE}	Rise time(1)	C_{OUT} = 1 nF		750	1250	ns
t_{FALL}	Fall time(1)	C_{OUT} = 1 nF		250	500	
LINEAR CURRENT AMPLIFIER						
V_{IO}	Input offset voltage		−15	0	15	mV
	Voltage gain		60	80		dB
V_{IMAX}	IMAX control voltage	V_{IMAX} = V_{OUT}, V_{SENSE} = V_{VCC}, wrt VCC	−20	0	20	mV
		V_{IMAX} = V_{OUT}, V_{SENSE} = V_{REF}, wrt REF	−20	0	20	
	SENSE input bias			1.5	3.5	µA
SHUTDOWN						
	Shutdown threshold voltage		0.6	1.5	2.0	V
	input current	$\overline{SD}$ = 5 V		150	300	µA
	Delay to output time(1)			0.5	2.0	µs

(1) Ensured by design. Not production tested.
(2) A mathematical averaging is used to determine this value. See Application Section for more information.

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ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C for the UC3914, −40°C to 85°C for the UC2914, V_{CC} = 12V, V_{PUMP} = $V_{PUMP(max)}$, $\overline{SD}$ = 5 V, C_{P1} = C_{P2} = C_{PUMP}= 0.01 µF. T_A = T_J. (Unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGE PUMP						
f_{OSC}, f_{OSCB}	Oscillator frequency	OSC, OSCB	60	150	250	kHz
V_{OH}	High-level output voltage	I_{OSC} = −5 mA	10.0	11.0	11.6	V
V_{OL}	Low-level output voltage	I_{OSC} = 5 mA		0.2	0.5	V
	Output clamp voltage	V_{CC} = 25 V	18.5	20.5	22.5	V
I_{LIM}	Output current limit	High side only	−20	−10	−3	mA
	Pump diode voltage drop	I_{DIODE} = 10 mA, measured from PMP to PMPB, PMPB to VPUMP	0.5	0.9	1.3	V
	PMP clamp voltage	V_{CC} = 25 V	18.5	20.5	22.5	V
	VPUMP maximum voltage	V_{VOUTS} = V_{CC} charge pump disable threshold, V_{CC} = 12 V	20	22	24	V
		V_{VOUTS} = V_{CC} charge pump disable threshold, V_{CC} = 35 V	42	45	48	V
	VPUMP hysteresis	V_{VOUTS} = V_{CC} charge pump re-enable threshold, V_{CC} = 12 V	0.3	0.7	1.4	V
		V_{VOUTS} = V_{CC} charge pump re-enable threshold, V_{CC} = 35 V	0.25	0.70	1.40	V
REFERENCE						
	REF output voltage	wrt VCC	−2.25	−2.00	−1.75	V
	REF current limit		12.5	20.0	50.0	mA
	Load regulation	1 mA ≤ I_{VREF} ≤ 5 mA		25	60	mV
	Line regulation	5 V ≤ V_{VCC} ≤ 35 V		25	100	mV
FAULT						
	Low-level output voltage	I_{FAULT} = 1 mA		100	200	mV
	Output leakage	V_{FAULT} = 35 V		10	500	nA
LATCH						
	Latch release threshold voltage	High-to-low	0.6	1.4	2.0	V
	Input current	V_{LR} = 5 V		500	750	µA
POWER LIMITING						
	Duty cycle control	I_{PLIM} = 200 µA In fault mode	0.6%	1.3%	2.0%	
		I_{PLIM} = 3 mA In fault mode	0.05%	0.12%	0.20%	
OVERLOAD						
	Delay-to-output time(1)			500	1250	ns
	Threshold voltage	wrt IMAX	−250	−200	−150	mV

(1) Ensured by design. Not production tested.

(2) A mathematical averaging is used to determine this value. See Application Section for more information.

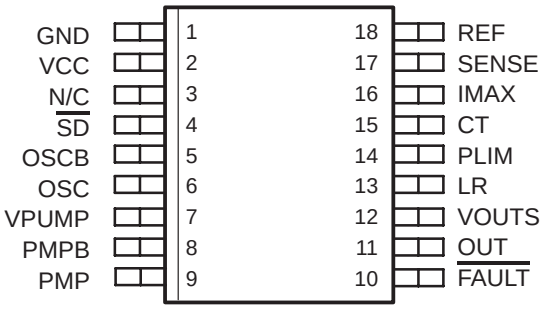
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AVAILABLE OPTIONS

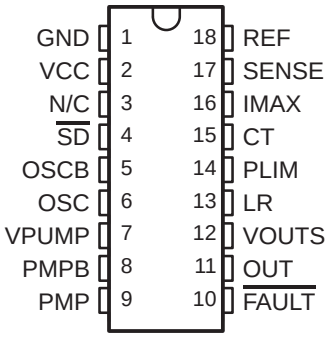
T_A	PACKAGED DEVICES	
	PLASTIC DIL−18 (N)	PLASTIC SOIC (DW)(1)
−40°C to 85°C	UC2914N	UC2914DW
0°C to 70°C	UC3914N	UC3914DW

(1) The DW package is available taped and reeled. Add an TR suffix to the device type (e.g. UC2914DWTR) to order quantities of 2,000 devices per reel.

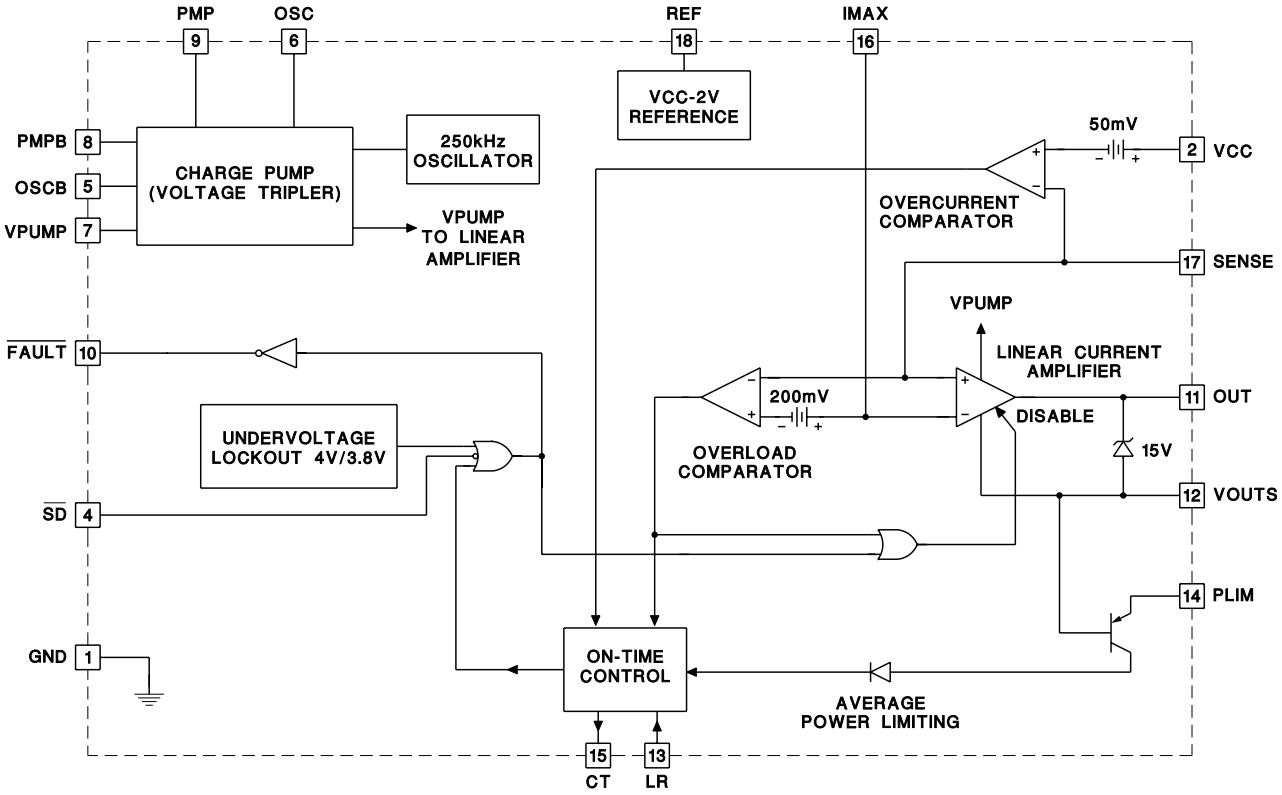
SOIC−18
DW PACKAGE
(TOP VIEW)



DIL−18
N PACKAGE
(TOP VIEW)



BLOCK DIAGRAM



UDG−95134−2

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TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CT	15	I/O	A capacitor is connected to this pin in order to set the maximum fault time. The minimum fault time must be more than the time to charge external load capacitance. The fault time is defined as shown in equation (1) where I_{CH} = 100 μA + I_{PL}, where I_{PL} is the current into the power limit pin. Once the fault time is reached the output shuts down for a time given by equation (2) where I_{DIS} is nominally 3 μA..
$\overline{\text{FAULT}}$	10	O	Open collector output which pulls low upon any of the following conditions: timer fault, shutdown, UVLO. This pin MUST be pulled up to V_{VCC} or another supply through a suitable impedance.
GND	1	−	Ground reference for the device.
IMAX	16	I	This pin programs the maximum allowable sourcing current. Since REF is a −2-V reference (with respect to VCC), a voltage divider can be derived from VCC to REF in order to generate the program level for the IMAX pin. The current level at which the output appears as a current source is equal to the voltage on the IMAX pin, with respect to VCC, divided by the current sense resistor. If desired, a controlled current startup can be programmed with a capacitor on IMAX to VCC.
LR	13	I	If this pin is held high and a fault occurs, the timer is prevented from resetting the fault latch when CT is discharged below the reset comparator threshold. The part does not retry until this pin is brought to a logic low or a power-on-reset occurs. Pulling this pin low before the reset time is reached does not clear the fault until the reset time is reached. Floating or holding this pin low results in the part repeatedly trying to reset itself if a fault occurs.
OUT	11	O	Output drive to the MOSFET pass element. Internal clamping ensures that the maximum V_{GS} drive is 15 V.
OSC	6	O	Complementary output drivers for intermediate charge pump stages. A 0.01-μF capacitor should be placed between OSC and PMP, and OSCB and PMPB.
OSCB	5	O	
PLIM	14	I	This feature ensures that the average MOSFET power dissipation is controlled. A resistor is connected from this pin to VCC. Current flows into PLIM, adding to the fault timer charge current, reducing the duty cycle from the typical 3% level. When I_{PL} >> 100 μA then the average MOSFET power dissipation is given by equation (3).
PMP	9	I	Complementary pins which couple charge pump capacitors to internal diodes and are used to provide charge to the reservoir capacitor tied to VPUMP. Typical capacitor values used are 0.01-μF.
PMPB	8	I	
REF	18	O	−2-V reference with respect to VCC used to program the IMAX pin voltage. A 0.1-μF ceramic or tantalum capacitor MUST be tied between this pin and VCC to ensure proper operation of the device.
$\overline{\text{SD}}$	4	I	When this TTL-compatible input is brought to a logic low, the output of the linear amplifier is driven low, $\overline{\text{FAULT}}$ is pulled low and the device is put into a low power mode. The ABSOLUTE maximum voltage that can be placed on this pin is 12 V.
SENSE	17	I	Input voltage from the current sense resistor. When there is greater than 50 mV on this pin with respect to VCC, a fault is sensed and CT begins to charge.
VCC	2	I	Input voltage to the device. The voltage range is from 4.5 V to 35 V. The minimum input voltage required for operation is 4.5 V.
VOUTS	12	O	Source connection of external N-channel MOSFET and sensed output voltage of load.
VPUMP	7	O	Charge pump output voltage. A capacitor should be tied between this pin and VOUTS with a typical value being 0.01-μF.

$$T_{FAULT} = \frac{2 \times C_T}{I_{CH}} \quad (1)$$

$$T_{SD} = \frac{2 \times C_T}{I_{DIS}} \quad (2)$$

$$P_{FET(avg)} = I_{MAX} \times 3 \times 10^{-6} \times R_{PL} \quad (3)$$

APPLICATION INFORMATION

The UC3914 is to be used in conjunction with external passive components and an N-channel MOSFET to facilitate hot swap capability of application modules. A typical application setup is given in Figure 1.

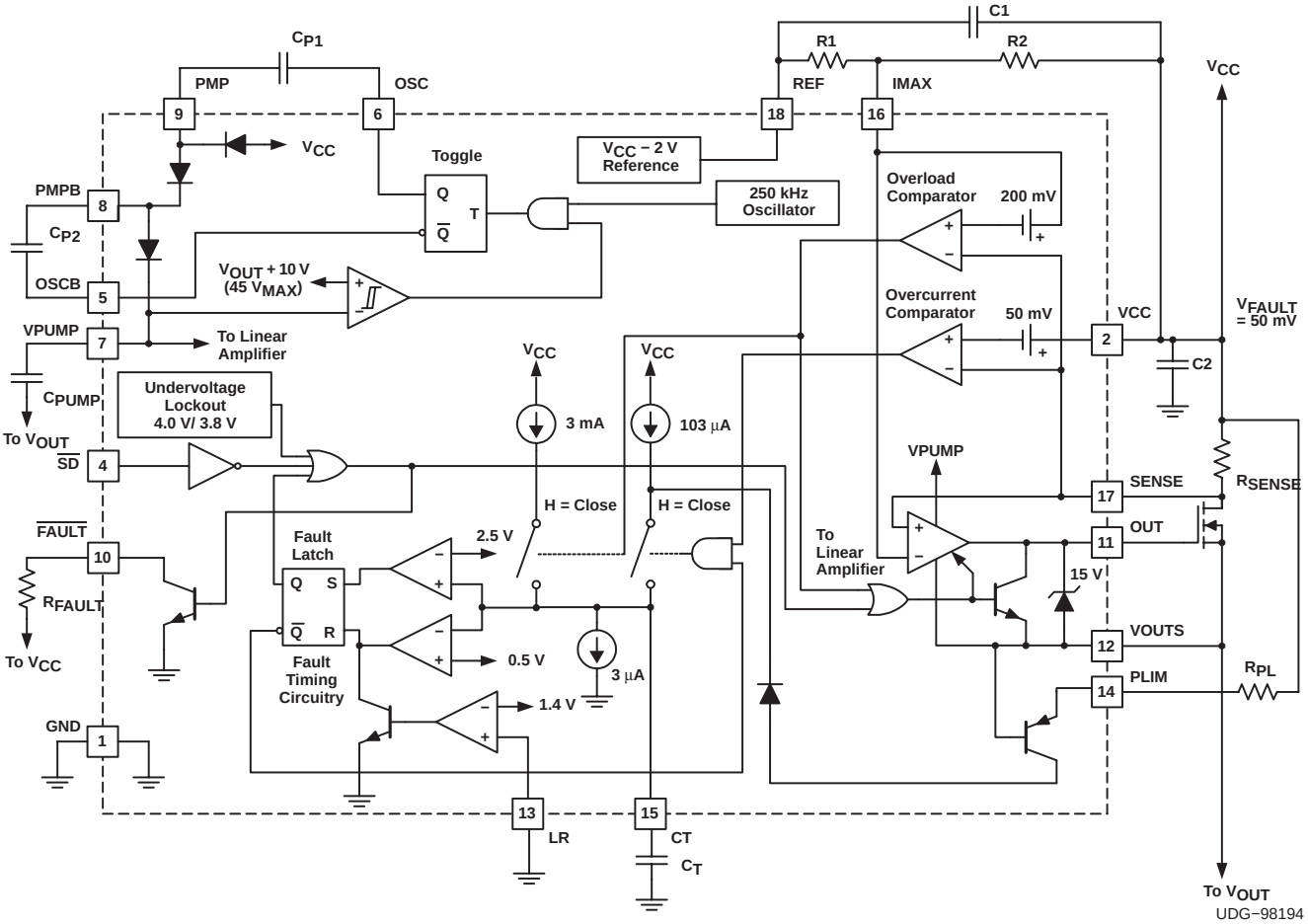


Figure 1. Typical Application

The term *hot swap* refers to the system requirement that submodules be swapped in or out upon failure or system modification without removing power to the operating hardware. The integrity of the power bus must not be compromised due to the addition of an unpowered module. Significant power bus glitches can occur due to the substantial initial charging current of on-board module bypass capacitance and other load conditions (for more information on hot swapping and power management applications, see SLUA157). The UC3914 provides protection by monitoring and controlling the output current of an external N-channel MOSFET to charge this capacitance and provide load current. The addition of the N-channel MOSFET, a sense resistor, R_{SENSE}, and two other resistors, R1 and R2, sets the programmed maximum current level the N-channel MOSFET can source to charge the load in a controlled manner. The equation for this current, I_{MAX}, is:

$$I_{MAX} = \frac{V_{VCC} - V_{IMAX}}{R_{SENSE}} \quad (4)$$

where

- V_{IMAX} is the voltage generated at the IMAX pin

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APPLICATION INFORMATION

Analysis of the application circuit shows that V_{IMAX} (with respect to GND) can be defined as:

$$V_{IMAX} = V_{REF} + \frac{(V_{CC} - V_{REF}) \times R1}{R1 + R2} = \frac{2V \times R1}{R1 + R2} + V_{REF} \quad (5)$$

where

- V_{REF} is the voltage on the REF pin, an internally generated potential 2-V below VCC

The UC3914 also has an internal overcurrent comparator which monitors the voltage between SENSE and VCC. If this voltage exceeds 50 mV, the comparator determines that a fault has occurred, and a timing capacitor, CT, begins to charge. This can be rewritten as a current which causes a fault, I_{FAULT}:

$$I_{FAULT} = \frac{50\ mV}{R_{SENSE}} \quad (6)$$

FAULT TIMING

Figure 2 shows the circuitry associated with the fault timing function of the UC3914. A typical fault mode, where the overload comparator and current source I3 do not factor into operation (switch S2 is open), is first considered. Once the voltage across R_{SENSE} exceeds 50 mV, a fault has occurred. This causes the timing capacitor, C_T, to charge with a combination of 100 μA (I1) plus the current from the power limiting circuitry (I_{PL}).

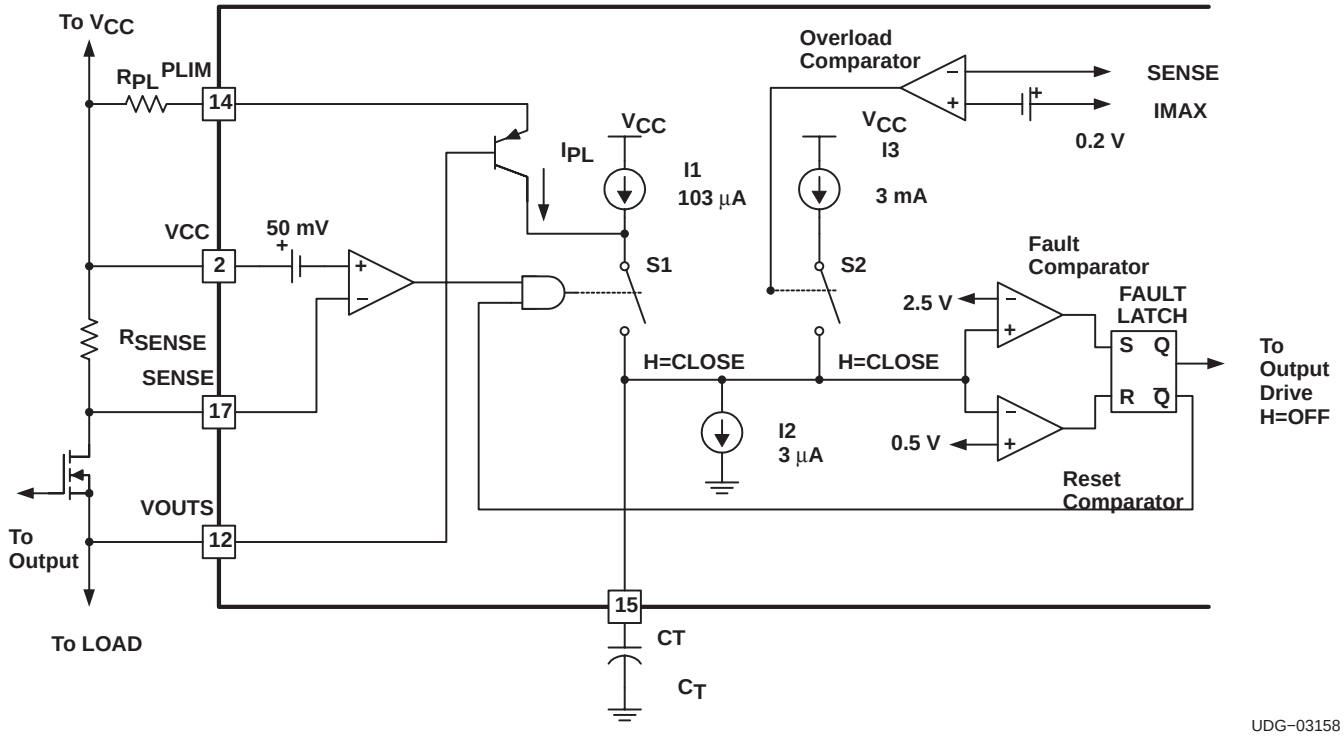


Figure 2. Fault Timing Circuitry Including Power Limit and Overcurrent

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APPLICATION INFORMATION

Figure 3 shows typical fault timing waveforms for the external N-channel MOSFET output current, the voltage on the CT pin, and the output load voltage, V_{OUT}, with LR left floating or grounded.

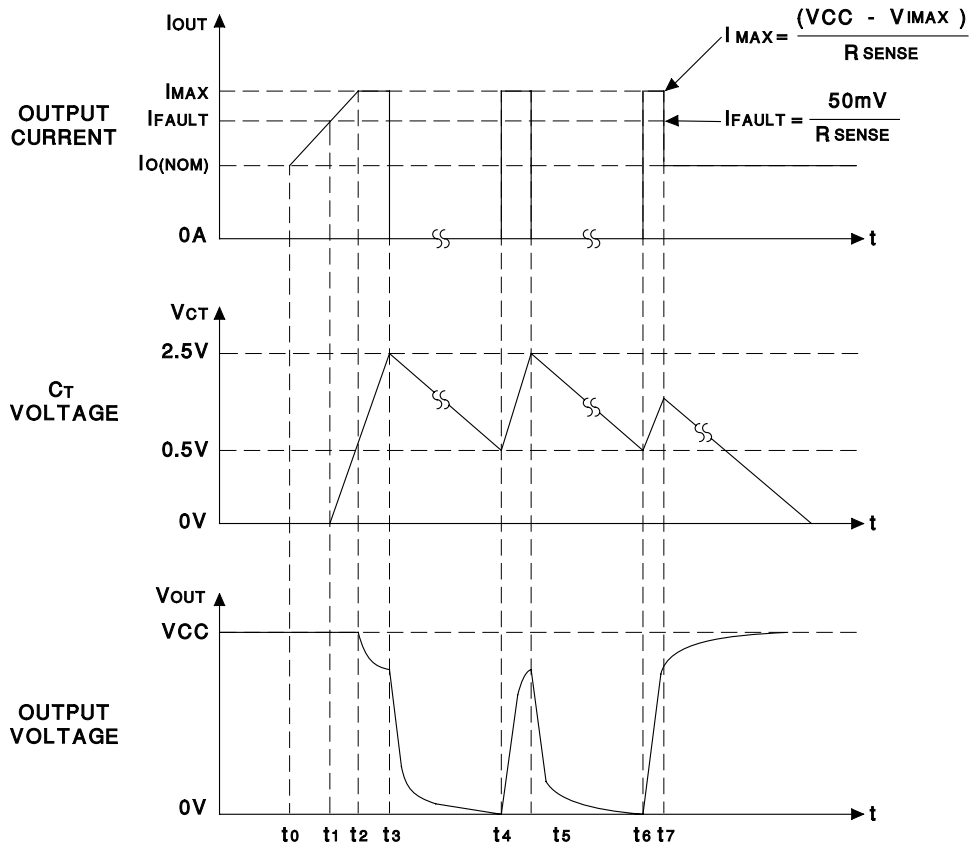


Figure 3. Typical Timing Diagram

Table 1. Fault Timing Conditions

TIME	CONDITION
t0	Normal conditions. Output current is nominal, output voltage is at positive rail, VCC
t1	Fault control reached. Output current rises above the programmed fault value, C_T begins to charge at 100-µA + I_{PL}.
t2	Maximum current reached. Output current reaches the programmed maximum level and becomes a constant current with value IMAX.
t3	Fault occurs. C_T has charged to 2.5 V, fault output goes low, the FET turns off allowing no output current to flow, V_{VOUTS} discharges to GND.
t4	Retry. C_T has discharged to 0.5 V, but fault current is still exceeded, C_T begins charging again, FET is on, V_{OUT} increases.
t5 = t3	Illustrates < 3% duty cycle depending upon R_{PL} selected.
t6=t4	
t7=t0	Fault released, normal condition. Return to normal operation of the load.

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APPLICATION INFORMATION

The output voltage waveforms have assumed an R-C characteristic load and time constants vary depending upon the component values. Prior to time t0, the load is fully charged to almost V_{VCC} and the N-channel MOSFET is supplying the current, I_{OUT}, to the load. At t0, the current begins to ramp up due to a change in the load conditions until, at t1, the fault current level, I_{FAULT}, has been reached to cause switch S1 to close. This results in C_T being charged with the current sources I1 and I_{PL}. During this time, V_{OUT} remains almost equal to V_{VCC} except for small losses from voltage drops across the sense resistor and the N-channel MOSFET. The output current reaches the programmed maximum level, I_{MAX}, at t2. The CT voltage continues to rise since I_{MAX} is still greater than I_{FAULT}. The load output voltage drops because the current load requirements have become greater than the controlled maximum sourcing current. The CT voltage reaches the upper comparator threshold (Figure 2) of 2.5 V at t3, which promptly shuts off the gate drive to the N-channel MOSFET (not shown but can be inferred from the fact that no output current is provided to the load), latches in the fault and opens switch S1 disconnecting the charging currents I1 and I_{PL} from CT.

Since no output current is supplied, the load voltage decays at a rate determined by the load characteristics and the capacitance. The 3-µA current source, I2, discharges C_T to the 0.5-V reset comparator threshold. This time is significantly longer than the charging time and is the basis for the duty cycle current limiting technique. When the CT voltage reaches 0.5 V at t4, the part performs a retry, allowing the N-channel MOSFET to again source current to the load and cause VOUT to rise. In this particular example, IMAX is still sourced by the N-channel MOSFET at each attempted retry and the fault timing sequence is repeated until time t7 when the load requirements change to I_{OUT}. Since I_{OUT} is less than the fault current level at this time, switch S1 is opened, I2 discharges C_T and V_{OUT} rises almost to the level of VCC.

Figure 4 shows fault timing waveforms similar to those depicted in Figure 3 except that the latch reset (LR) function is utilized. Operation is the same as described above until t4 when the voltage on CT reaches the reset threshold. Holding LR high prevents the latch from being reset, preventing the device from performing a retry (sourcing current to the load). The UC3914 is latched off until either LR is pulled to a logic low, or the chip is forced into an under voltage lockout (UVLO) condition and back out of UVLO causing the latch to automatically perform a power on reset. Figure 4 illustrates LR being toggled low at t5, causing the part to perform a retry. Time t6 again illustrates what happens when a fault is detected. The LR pin is toggled low and back high at time t7, prior to the voltage on the CT pin hitting the reset threshold. This information tells the UC3914 to allow the part to perform a retry when the lower reset threshold is reached, which occurs at t8. Time t9 corresponds to when load conditions change to where a fault is not present as described for Figure 3.

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APPLICATION INFORMATION

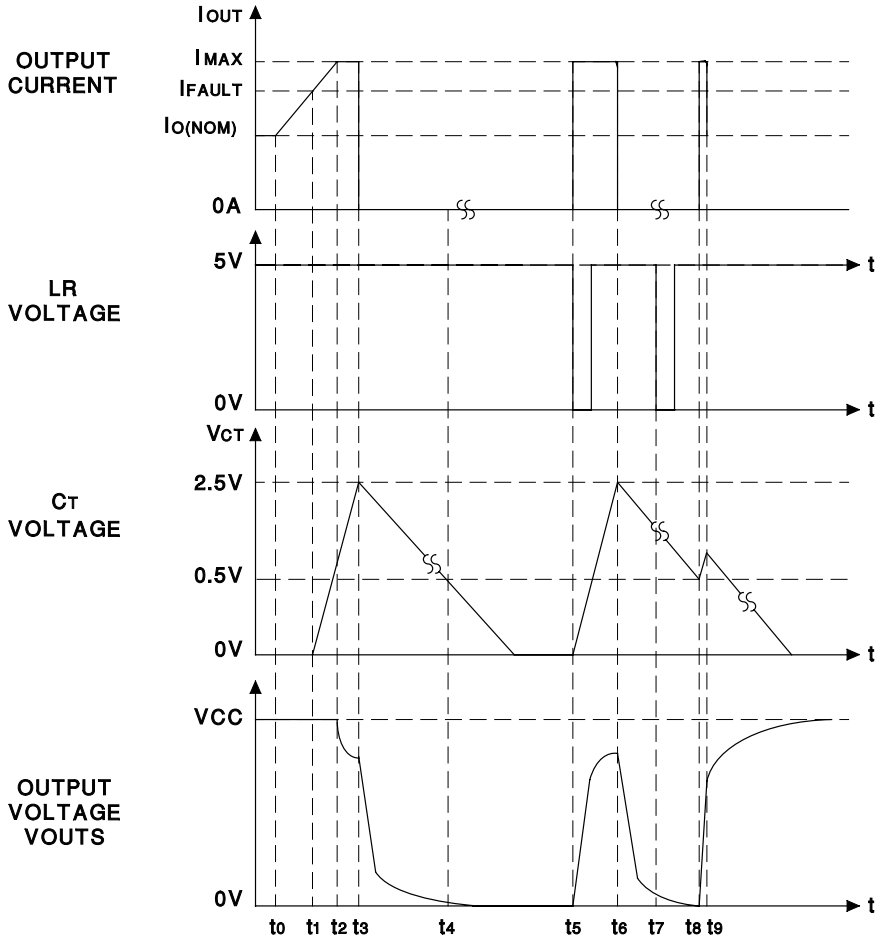


Figure 4. Typical Timing Diagram Using Latch Reset (LR) Function

Table 2. Fault Timing Conditions with Latch Reset Function

TIME	CONDITION
t0	Normal conditions. Output current is nominal, output voltage is at positive rail, VCC
t1	Fault control reached. Output current rises above the programmed fault value, C_T begins to charge at 100-µA + I_{PL}.
t2	Maximum current reached. Output current reaches the programmed maximum level and becomes a constant current with value IMAX.
t3	Fault occurs. C_T has charged to 2.5 V, fault output goes low, the FET turns off allowing no output current to flow, V_{VOUTS} discharges to GND.
t4	Reset comparator threshold reached but no retry since LR pin held high.
t5	LR toggled low, N-channel MOSFET turned on and sources current to load.
t6=t3	
t7	LR toggled low before V_{CT} reaches reset comparator threshold, causing retry.
t8	Since LR toggled low during present cycle, N-channel MOSFET turned on and sources current to load.
t9=t0	Fault released, normal condition. Return to normal operation of the load.

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APPLICATION INFORMATION

Power Limiting

The power limiting circuitry is designed to only source current into the CT pin. To implement this feature, a resistor, R_{PL}, should be placed between VCC and PLIM. The current, I_{PL} (show in Figure 2) is given by the following expression:

$$I_{PL} = \frac{V_{VCC} - V_{VOUTS}}{R_{PL}}, \text{ for } V_{VOUTS} > 1\ V + V_{CT} \tag{7}$$

where

- V_{CT} is the voltage on the CT pin

For $V_{VOUTS} < 1\ V + V_{CT}$ the common mode range of the power limiting circuitry causes $I_{PL} = 0$ A leaving only the 100-μA current source to charge C_T. $V_{VCC} - V_{VOUTS}$ represents the voltage across the N-channel MOSFET pass device.

This feature limits average power dissipation in the pass device. Note that under a fault condition where the output current is just above the fault level, but less than the maximum level, $V_{VOUTS} \sim V_{VCC}$, $I_{PL} = 0$ A and the C_T charging current is 100 μA.

During a fault, the CT pin charges at a rate determined by the internal charging current and the external timing capacitor, C_T. Once C_T charges to 2.5 V, the fault comparator trips and sets the fault latch. When this occurs, OUT is pulled down to VOUTS, causing the external N-channel MOSFET to shut off and the charging switch, S1, to open. C_T is discharged with I2 until the V_{CT} potential reaches 0.5 V. Once this occurs, the fault latch resets (unless LR is being held high, whereby a fault can only be cleared by pulling this pin low or going through a power-on-reset cycle), which re-enables the output of the linear amplifier and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the overcurrent comparator closes the charging switch causing the cycle to repeat. Under a constant fault the duty cycle is given by:

$$\text{Duty Cycle} = \frac{3\ \mu A}{I_{PL} + 100\ \mu A} \tag{8}$$

Average power dissipation can be limited using the PLIM pin. Average power dissipation in the pass element is given by:

$$P_{FET(avg)} = \left(V_{VCC} - V_{VOUTS}\right) \times I_{MAX} \times \text{Duty Cycle} \tag{9}$$

$$= \left(V_{VCC} - V_{VOUTS}\right) \times I_{MAX} \times \frac{3\ \mu A}{I_{PL} + 100\ \mu A}$$

$V_{VCC} - V_{VOUTS}$ is the drain to source voltage across the MOSFET. When $I_{PL} >> 100\ \mu A$, the duty cycle equation given above can be rewritten as:

$$\text{Duty Cycle} = \frac{R_{PL} \times 3\ \mu A}{\left(V_{VCC} - V_{VOUTS}\right)} \tag{10}$$

and the average power dissipation of the MOSFET is given by:

$$P_{FET(avg)} = \left(V_{VCC} - V_{VOUTS}\right) \times I_{MAX} \times \frac{R_{PL} \times 3\ \mu A}{\left(V_{VCC} - V_{VOUTS}\right)} = I_{MAX} \times R_{PL} \times 3\ \mu A \tag{11}$$

The average power is limited by the programmed I_{MAX} current and the appropriate value for R_{PL}.

PRODUCT PREVIEW

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OVERLOAD COMPARATOR

The linear amplifier in the UC3914 ensures that the external N-channel MOSFET does not source more than the current I_{MAX}, defined in equation (4):

$$I_{MAX} = \frac{V_{VCC} - V_{IMAX}}{R_{SENSE}}$$

In the event that output current exceeds the programmed IMAX current by more than 200-mV/R_{SENSE}, the output of the linear amplifier is immediately pulled low (with respect to VOUTS) providing no gate drive to the N-channel MOSFET, and preventing current from being delivered to the load. This situation could occur if the external N-channel MOSFET is not responding to a command from the UC3914 or output load conditions change quickly to cause an overload condition before the linear amplifier can respond. For example, if the N-channel MOSFET is sourcing current into a load and the load suddenly becomes short circuited, an overload condition may occur. The short circuit causes the V_{GS} of the N-channel MOSFET to immediately increase, resulting in increased load current and voltage drop across R_{SENSE}. If this drop exceeds the overload comparator threshold, the amplifier output is quickly pulled low. It also causes the CT pin to begin charging with I3, a 3-mA current source (refer to Figure 2) and continue to charge until approximately 1-V below V_{VCC}, where it is clamped. This allows a constant fault to show up on $\overline{\text{FAULT}}$ and since the voltage on CT charges past 2.5 V only in an overload fault condition, it can be used for detection of output N-channel MOSFET failure or to build redundancy into the system.

ESTIMATING MINIMUM TIMING CAPACITANCE

The startup time of the device may not exceed the fault time for the application. Since the timing capacitor, C_T, determines the fault time, its minimum value can be determined by calculating the startup time of the device. The startup time is dependent upon several external components. A load capacitor, C_{LOAD}, should be tied between VOUTS and GND. Its value should be greater than that of C_{PUMP}, the reservoir capacitor tied from VPUMP to VOUTS (see Figure 4). Given values of C_{LOAD}, R_{LOAD}, R_{SENSE}, V_{VCC} and the resistors determining the voltage on IMAX, the user can calculate the approximate startup time of the node V_{OUT}. This time must be less than the time it takes for CT to charge to 2.5 V. Assuming the user has determined the fault current, R_{SENSE} can be calculated by:

$$R_{SENSE} = \frac{50\ mV}{I_{FAULT}} \tag{12}$$

I_{MAX} is the maximum current the UC3914 allows through the transistor, M1. During startup with an output capacitor, M1 can be modeled as a constant current source of value I_{MAX} using equation (4).

Given this information, calculation of startup time is now possible via the following:

Using a constant-current load model, use this equation:

$$T_{START} = \frac{\left(C_{LOAD} \times V_{VCC}\right)}{\left(I_{MAX} - I_{LOAD}\right)} \tag{13}$$

Using a resistive load model, use this equation:

$$T_{START} = -R_{LOAD} \times C_{LOAD} \times \ell n\left(1 - \frac{V_{VCC}}{I_{MAX} \times R_{LOAD}}\right) \tag{14}$$

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The only remaining external component which may affect the minimum timing capacitor is the optional power limiting resistor, R_{PL}. If the addition of R_{PL} is desirable, its value can be determined from the *Power Limiting* section of this datasheet. The minimum timing capacitor values are now given by the following equations.

Using a constant-current load model, use this equation:

$$CT_{min} = T_{START} \times \left[\frac{10^{-4} \times R_{PL} + \left(\frac{V_{VCC}}{2} \right)}{2 \times R_{PL}} \right] \quad (15)$$

Using a resistive load model, use this equation:

$$CT_{(min)} = \frac{\left(10^{-4} \times R_{PL} + V_{VCC} - \left(I_{MAX} \times R_{LOAD}\right)\right) \times T_{START}}{2 \times R_{PL}} + \frac{V_{VCC}}{2 \times R_{PL}} \times R_{LOAD} \times C_{LOAD} \quad (16)$$

OUTPUT CURRENT SOFTSTART

The external MOSFET output current can be increased at a user-defined rate to ensure that the output voltage comes up in a controlled fashion by adding capacitor C_{SS}, as shown in Figure 5. The one constraint that the UC3914 places on the soft-start time is that the charge pump time constant must be much less than the soft-start time constant to ensure proper soft-start operation. The time constant determining the startup time of the charge pump is given by:

$$\tau_{CP} = R_{OUT} \times C_{PUMP} \quad (17)$$

R_{OUT} is the output impedance of the charge pump given by:

$$R_{OUT} = \frac{1}{f_{PUMP} \times C_P} \quad (18)$$

where f_{PUMP} is the charge pump frequency (125 kHz) and $C_P = C_{P1} = C_{P2}$ are the charge pump flying capacitors. For typical values of C_{P1}, C_{P2} and C_{PUMP} (0.01-µF) and a switching frequency of 125 kHz, the output impedance is 800 Ω and the charge pump time constant is 8 µs. The charge pump should be close to being fully charged in 3 time constants or 24 µs. By placing a capacitor from VCC to IMAX, the voltage at IMAX, which sets the maximum output current of the MOSFET, exponentially decays from VCC to the desired value set by R1 and R2. The output current of the MOSFET is controlled via soft-start as long as the soft-start time constant (τ_{SS}) is much greater than the charge pump time constant τ_{CP}, given by:

$$\tau_{SS} = (R1 \parallel R2) \times C_{SS} \quad (19)$$

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MINIMIZING TOTAL DROPOUT UNDER LOW VOLTAGE OPERATION

In a typical application, the UC3914 is used to control the output current of an external N-channel MOSFET during hot swapping situations. Once the load has been fully charged, the desired output voltage on the load, V_{OUT}, needs to be as close to VCC as possible to minimize total dropout. For a resistive load, R_{LOAD}, the output voltage is given by:

$$V_{OUT} = \frac{R_{LOAD}}{R_{LOAD} + R_{SENSE} + R_{DS(on)}} \times V_{VCC} \quad (20)$$

R_{SENSE} sets the fault current, I_{FAULT}. $R_{DS(on)}$, the on-resistance of the N-channel MOSFET, should be made as small as possible to ensure V_{OUT} is as close to VCC as possible. For a given N-channel MOSFET, the manufacturer specifies the $R_{DS(on)}$ for a certain V_{GS} (i. e., between 7 V to 10 V). The source potential of the N-channel MOSFET is V_{OUT}. In order to ensure sufficient V_{GS}, this requires the gate of the N-channel MOSFET, which is the output of the linear amplifier, to be many volts higher than V_{VCC}. The UC3914 provides the capability to generate this voltage through the addition of three capacitors, C_{P1}, C_{P2} and C_{PUMP} as shown in Figure 6. These capacitors should be used in conjunction with the complementary output drivers and internal diodes included on-chip to create a charge pump or voltage tripler. The circuit boosts V_{VCC} by utilizing capacitors C_{P1}, C_{P2} and C_{PUMP} in such a way that the voltage at VPUMP approximately equals three times the voltage at VCC minus five times the voltage drop of the diodes, almost tripling the input supply voltage to the device.

$$V_{VPUMP} = \left(3 \times V_{VCC}\right) - \left(5 \times V_{DIODE}\right) \quad (21)$$

On each complete cycle, C_{P1} is charged to approximately (V_{VCC} − V_{DIODE}) (unless VCC is greater than 15 V causing internal clamping to limit this charging voltage to about 13 V) when the output Q of the toggle flip-flop is low. When $\overline{Q}$ is transitioned low (and Q correspondingly is brought high), the negative side of C_{P2} is pulled to ground, and C_{P1} charges C_{P2} up to approximately:

$$V_{CP2} = \left(2 \times V_{VCC}\right) - \left(3 \times V_{DIODE}\right) \quad (22)$$

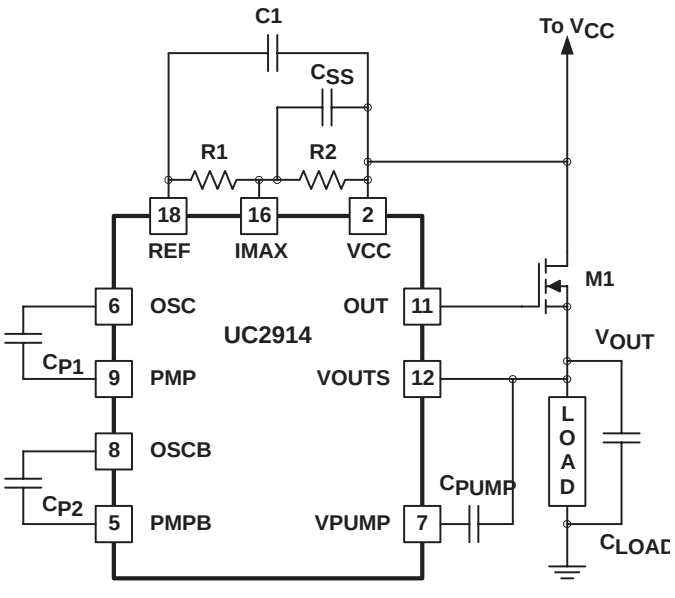


Figure 5. MOSFET Softstart Diagram

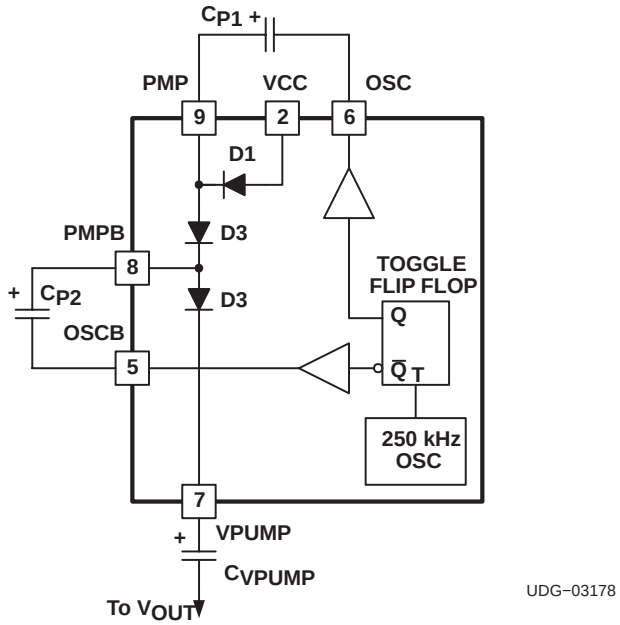


Figure 6. Charge Pump Block Diagram

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When $\overline{Q}$ is toggled high, the negative side of CP2 is brought to ($V_{CC} - V_{DIODE}$). Since the voltage across a capacitor cannot change instantaneously with time, the positive side of the capacitor swings up to:

$$V_{PMPB} = 3 \times V_{CC} - 4 \times V_{DIODE} \quad (23)$$

This charges C_{PUMP} up to:

$$V_{CPUMP} = 3 \times V_{CC} - 5 \times V_{DIODE} \quad (24)$$

The maximum output voltage of the linear amplifier is actually less than this because of the ability of the amplifier to swing to within approximately 1 V of V_{PUMP}. Due to inefficiencies of the charge pump, the UC3914 may not have sufficient gate drive to fully enhance a standard power MOSFET when operating at input voltages below 7 V. Logic level MOSFETs could be used depending on the application but are limited by their lower current capability. For applications requiring operation below 7 V, there are two ways to increase the charge pump output voltage. Figure 7 shows the typical tripler of Figure 6 enhanced with three external schottky diodes. Placing the schottky diodes in parallel with the internal charge pump diodes decreases the voltage drop across each diode thereby increasing the overall efficiency and output voltage of the charge pump.

Figure 8 shows a way to use the existing drivers with external diodes (or Schottky diodes for even higher pump voltages but with additional cost) and capacitors to make a voltage quadrupler. The additional charge pump stage provides a sufficient pump voltage to generate the maximum V_{GS}:

$$V_{VPUMP} = 4 \times V_{CC} - 7 \times V_{DIODE} \quad (25)$$

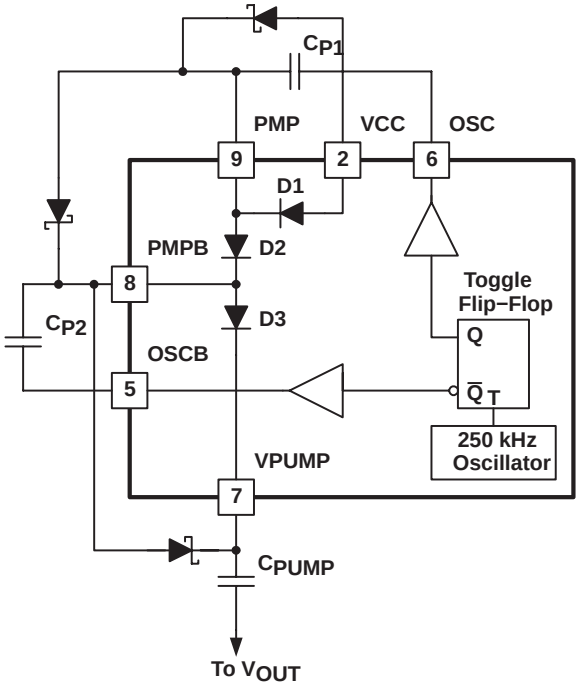


Figure 7. Enhanced Charge Pump

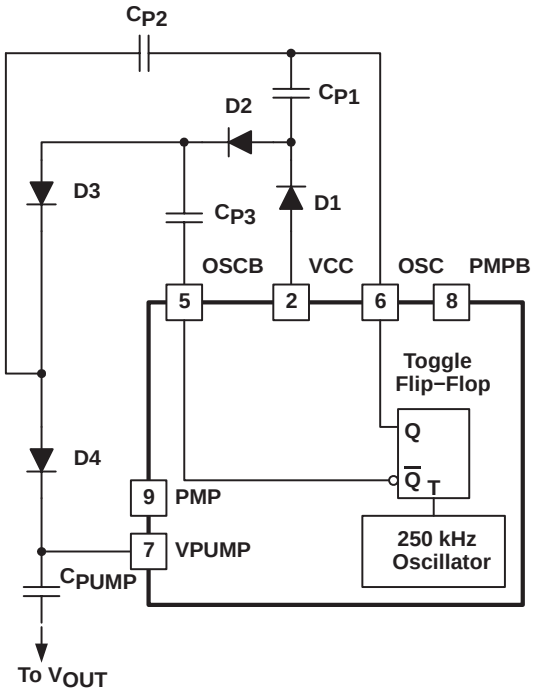


Figure 8. Low Voltage Operation to Produce Higher Pump Voltage

APPLICATION INFORMATION

Operation is similar to the case described above. This additional circuitry is not necessary for higher input voltages because the UC3914 has internal clamping which only allows V_{PUMP} to be 10 V greater than V_{VOUTS}.

Table 3 characterizes the UCx914 charge pump in its standard configuration, with external schottky diodes, and configured as a voltage quadrupler.

NOTE: The voltage quadrupler is unnecessary for input voltages above 7.0 V due to the internal clamping action.

Table 3. Charge Pump Characteristics

INPUT VOLTAGE (V_{CC})	INTERNAL DIODES (V_{GS})	EXTERNAL SCHOTTKY DIODES (V_{GS})	QUADRUPLER (V_{GS})
4.5	4.57	6.8	8.7
5.0	5.80	7.9	8.8
5.5	6.60	8.6	8.9
6.0	7.60	8.8	9.0
6.5	8.70	8.8	9.0
7.0	8.80	9.0	9.0
9.0	9.20	9.4	9.1
10.0	9.30	9.4	9.3

I_{CC} SPECIFICATIONS

The I_{CC} operating measurement is actually a mathematical calculation. The charge pump voltage is constantly being monitored with respect to both V_{CC} and V_{OUTS} to determine whether the pump requires servicing. If there is insufficient voltage on this pin, the charge pump drivers are alternately switched to raise the voltage of the pump (see Figure 9). Once the voltage on the pump is high enough, the drivers and other charge pump related circuitry are shutdown to conserve current. The pump voltage decays due to internal loading until it reaches a low enough level to turn the drivers back on. The chip requires significantly different amounts of current during these two modes of operation and the following mathematical calculation is used to calculate the average current:

$$I_{CC} = \frac{I_{CCdrivers(on)} \times T_{ON} + I_{CCdrivers(off)} \times T_{OFF}}{T_{ON} + T_{OFF}} \quad (26)$$

Since the charge pump does not always require servicing, the user may think that the charge pump frequency is much less than the datasheet specification. This is not the case as the free-running frequency is guaranteed to be within the datasheet limits. The charge pump servicing frequency can make it appear as though the drivers are operating at a much lower frequency

PRODUCT PREVIEW

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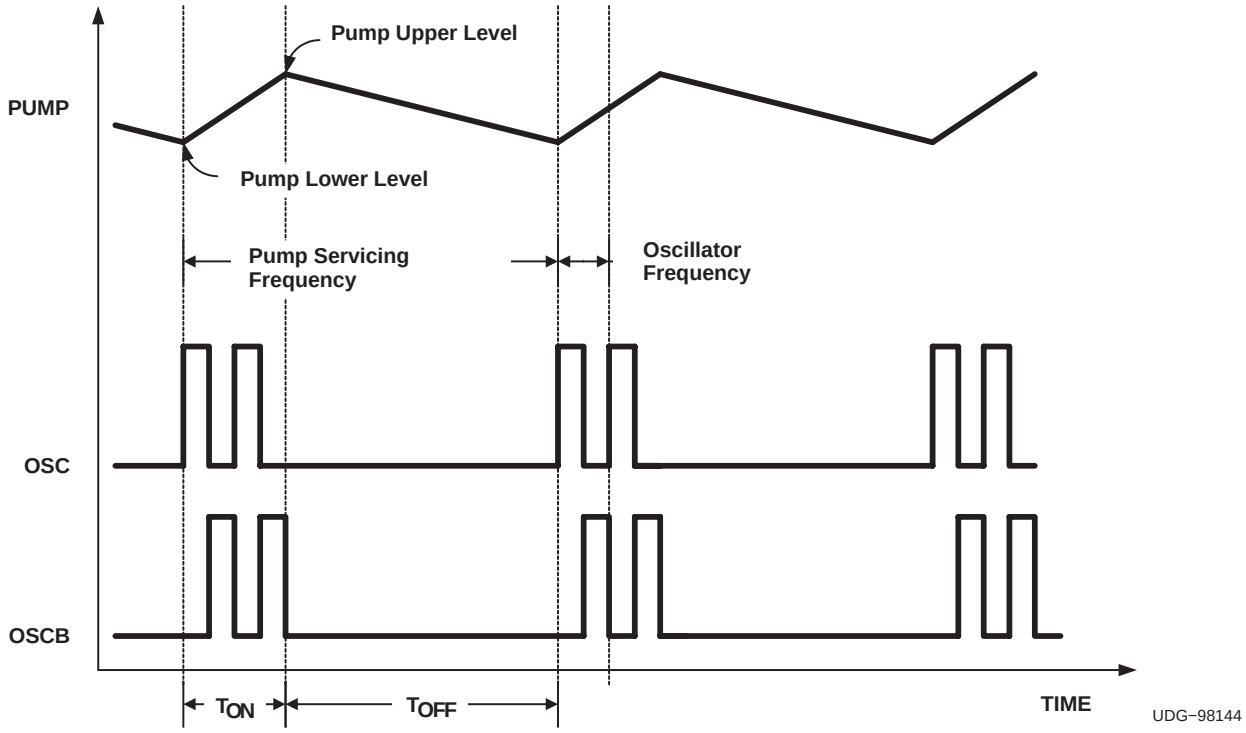


Figure 9. Charge Pump Waveforms

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

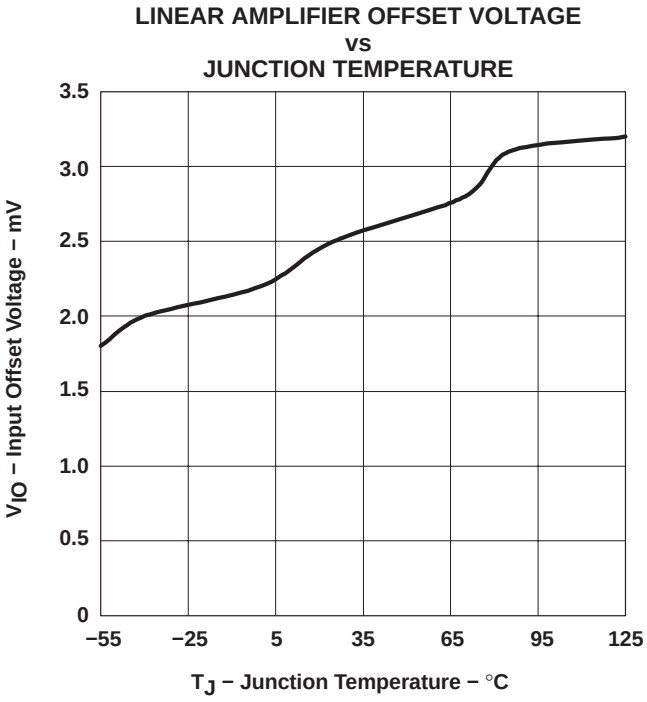


Figure 10

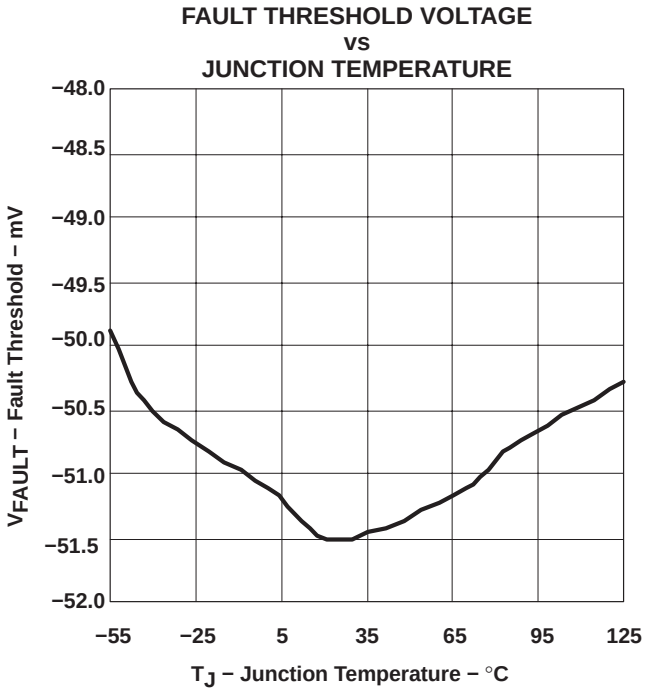


Figure 11

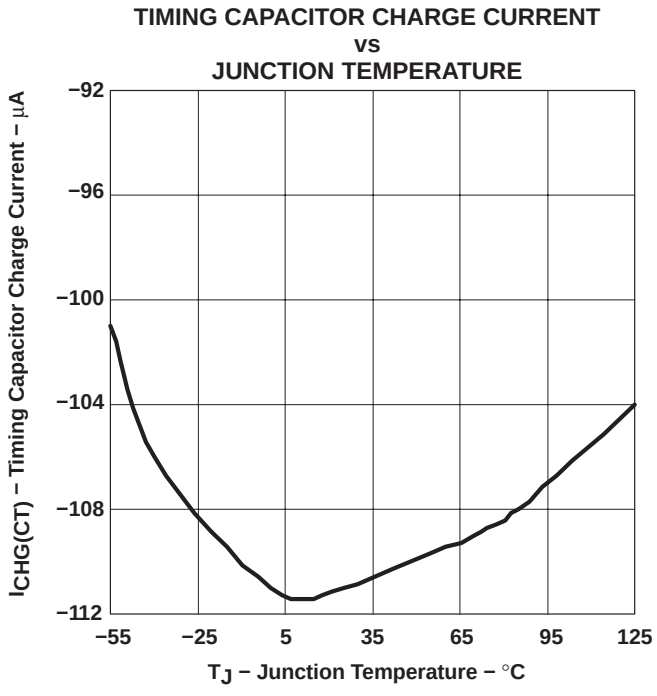


Figure 12

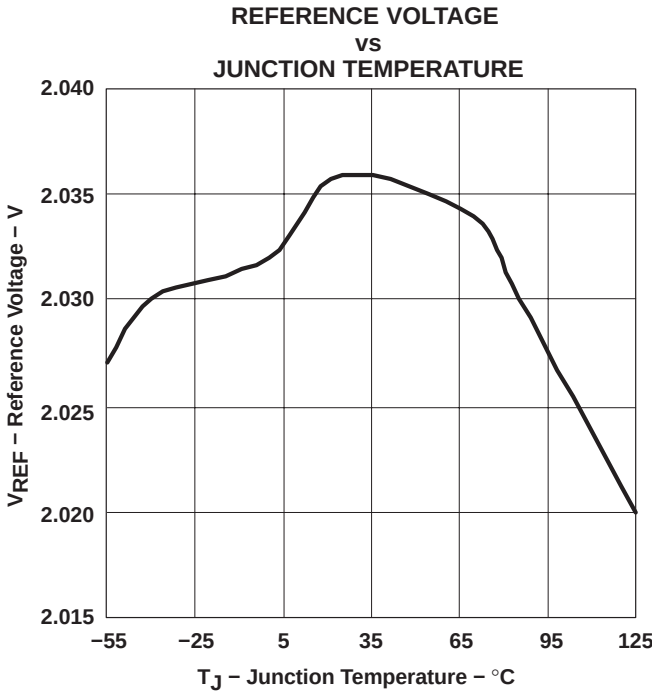


Figure 13

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

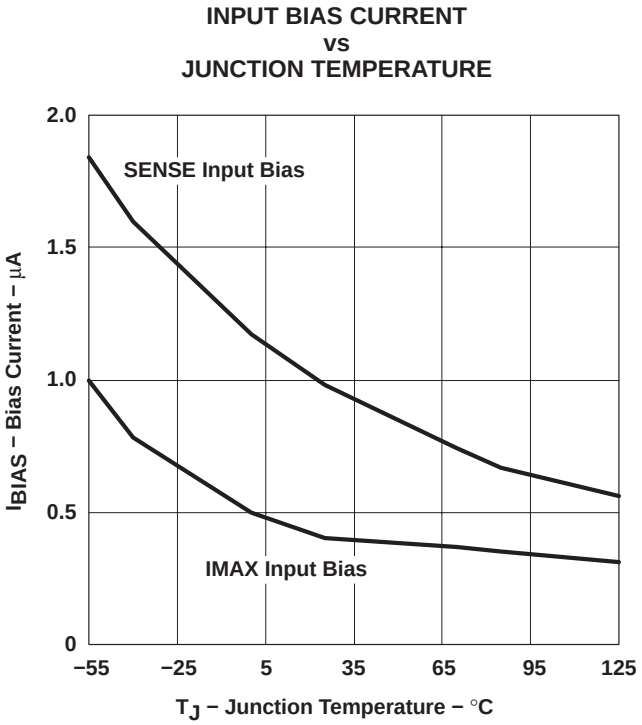


Figure 14

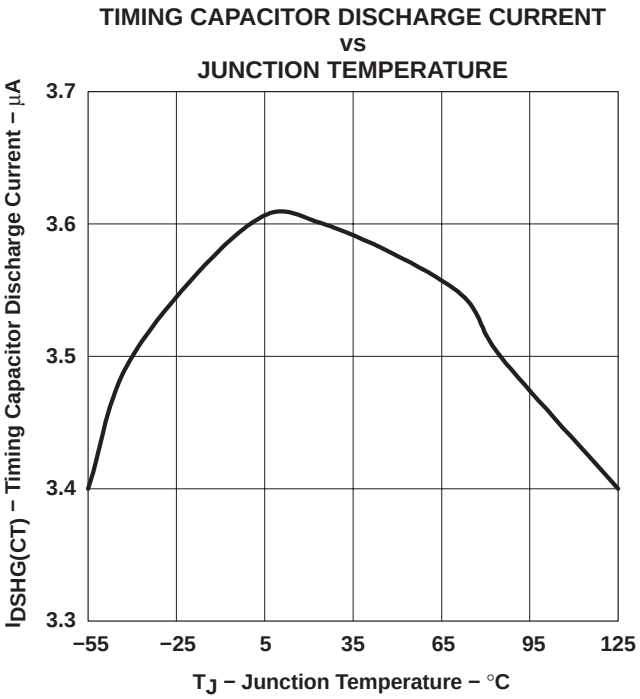


Figure 15

SAFETY RECOMMENDATIONS

Although the UC3914 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UC3914 is intended for use in safety critical applications where UL® or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UC3914 prevents the fuse from blowing in virtually all fault conditions, increasing system reliability and reducing maintainence cost, in addition to providing the hot swap benefits of the device.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2914DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2914DW	Samples
UC2914DWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2914DW	Samples
UC2914N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2914N	Samples
UC3914DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3914DW	Samples
UC3914DWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3914DW	Samples
UC3914DWTRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3914DW	Samples
UC3914N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3914N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

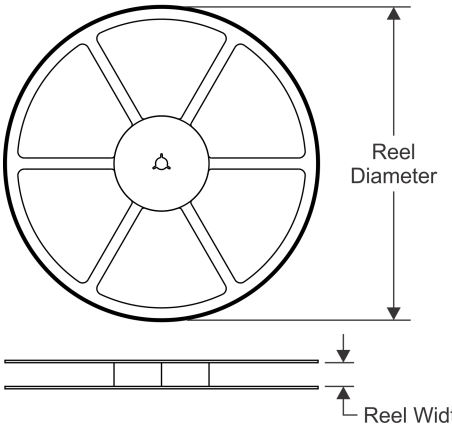
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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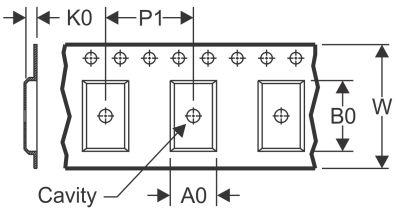
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

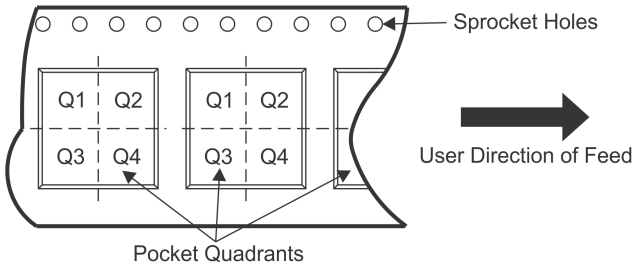


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

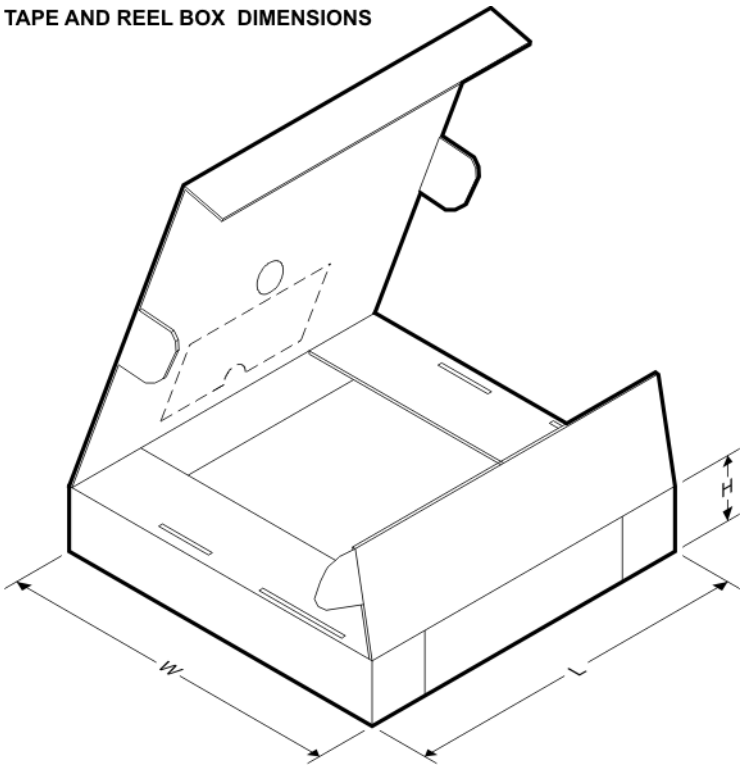
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2914DWTR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1
UC3914DWTR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1

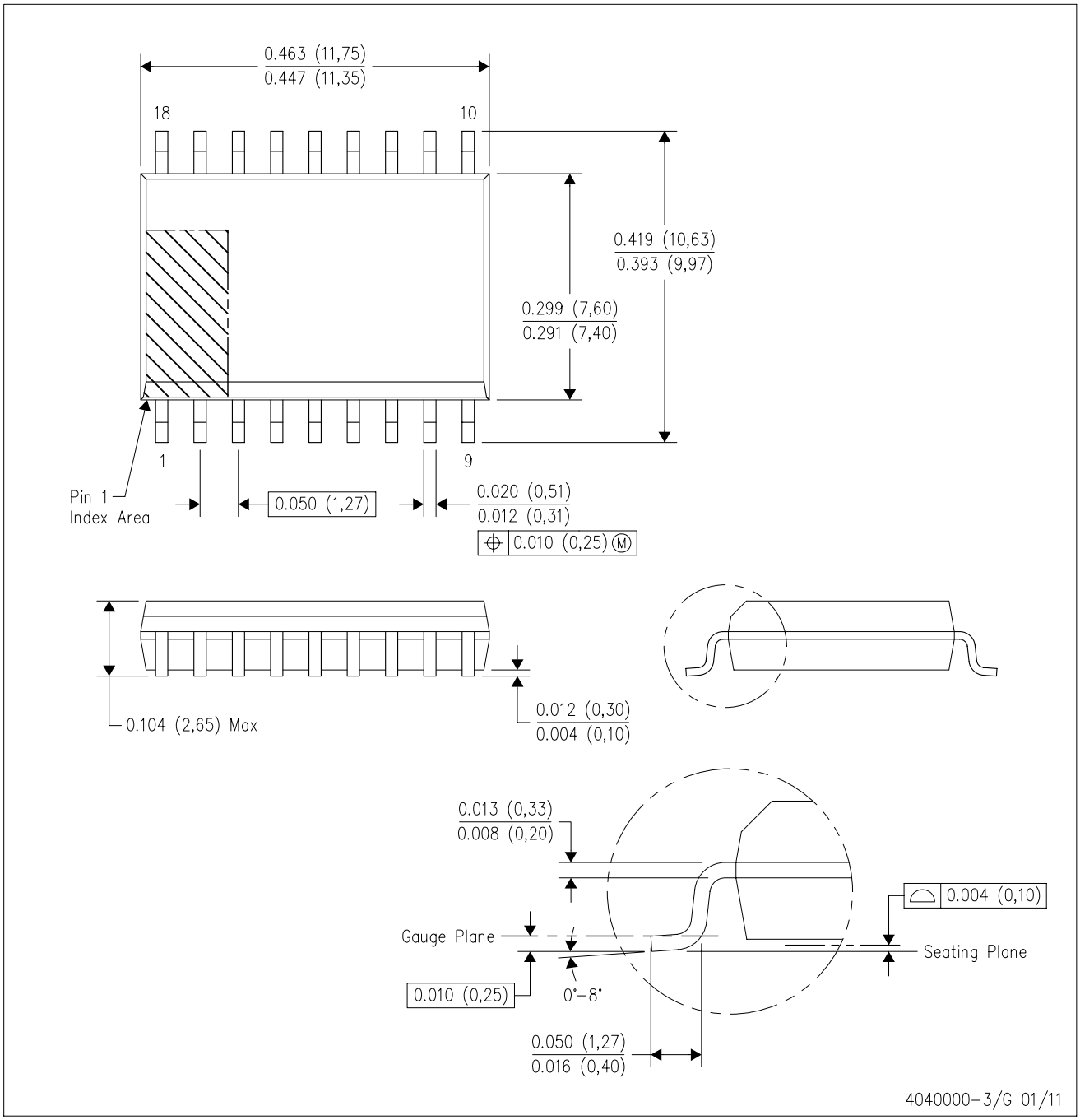
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

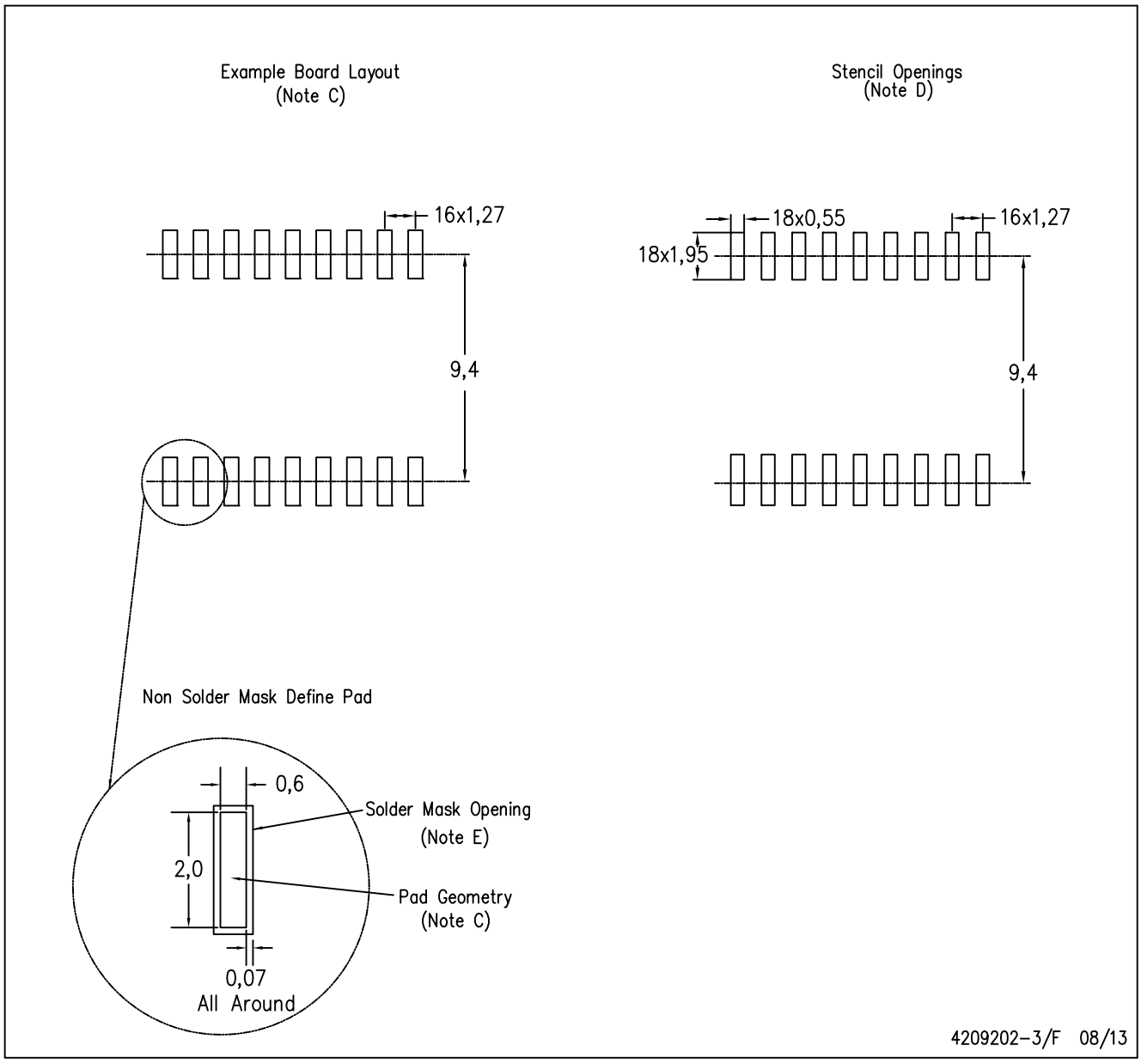
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2914DWTR	SOIC	DW	18	2000	367.0	367.0	45.0
UC3914DWTR	SOIC	DW	18	2000	367.0	367.0	45.0

DW (R–PDSO–G18) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AB.

DW (R–PDSO–G18) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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